IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of:	Group Art Unit: 2826
Michael G. KELLY	Examiner: Andujar, Leonardo
Application No.: 10/820,484	Docket No.: 10031133-1
Filed: April 8, 2004	Confirmation No.: 7400

For: **Thermal Dissipation In Integrated Circuit Systems**

APPEAL BRIEF

Mail Stop **Appeal Brief—Patent**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SMITH FROHWEIN TEMPEL
GREENLEE BLAHA LLC
Customer Number 35856

Sir:

This Appeal Brief is submitted further to the Notice of Appeal filed June 28, 2007. Also, the Notice of Panel Decision From Pre-Appeal Brief Review mailed February 15, 2008, indicating the panel's decision to have the case proceed to the Board of Patent Appeals and Interferences, is acknowledged. This Appeal Brief is filed within the one-month period for response set forth in that Notice.

The fee set forth in 37 C.F.R. § 41.20(b)(2) is submitted herewith. Any excess fees may be charged to, or any credits may be applied to, Deposit Account No. 50-3718.

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Date: March 12, 2008 /Lawrence D. Maxwell/
Lawrence D. Maxwell, Reg. No. 35,276

I. Real Party in Interest

The real party in interest is Avago Technologies General IP (Singapore) Pte. Ltd. (Company Registration No. 200512430D), a company incorporated under the laws of Singapore.

II. Related Appeals and Intereferences

Appellant is not aware of any related appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. Status of Claims

Claims 1-21 are pending. Each of claims 1-21 stands rejected. Appellant appeals all rejections of claims 1-21.

IV. Status of Amendments

No amendments have been filed following the final Office Action dated May 7, 2007.

V. Summary of Claimed Subject Matter

The invention as claimed in independent claim 1 is an integrated circuit system that includes a die that incorporates an integrated circuit and has a top side and a bottom side. The top side of the die supports an electrical signal communication metallization and a top side thermal dissipation metallization. The bottom side of the die supports a bottom side thermal dissipation metallization. (See page 1, line 30 – page 2, line 4; Figs. 1A-B and 2.)

In embodiments in accordance with the invention as claimed in claim 1, the top side thermal dissipation metallization and the bottom side thermal dissipation metallization provide high thermal conductivity paths for heat emanating from the integrated circuit die and robust attachments to an integrated circuit package in which the die may be mounted. In this way, the top side thermal dissipation metallization and the bottom side thermal dissipation metallization provide an effective way to remove heat from the integrated circuit die and maintain the temperature of the integrated circuit die within a reliable temperature range, while increasing the mechanical stability of the integrated circuit die and increasing the overall robustness of the final integrated circuit package in which the die may be mounted. In addition, the top side thermal dissipation metallization and the bottom side thermal dissipation metallization maybe formed using substrate-scale (e.g., wafer-scale) processing,

thereby increasing processing efficiency and allowing the integrated circuit die to be packaged using standard automatic metallurgical bonding equipment. (See page 3, lines 10-21.)

The specification defines the term "die" as a substrate that contains an integrated circuit" (see page 3, lines 23-24). The specification defines the term "metallization" as a "single-layer metal film or a multilayer metal film formed in or on an integrated circuit" (page 4, lines 3-4). Figures 1A and 1B show an embodiment of a die 10 that incorporates an integrated circuit 12 that constitutes an integrated circuit system in accordance with the invention defined in independent claim 1.

The die 10 has a top side 14 that supports an electrical signal communication metallization 18 and a top side thermal dissipation metallization 20. The top side thermal dissipation metallization 20 defines a thermal contact area on the top side 14 of die 10 that provides a high thermal conductivity path from the die 10 to, for example, a heat spreader of a package into which die 10 is to be mounted (see page 4, lines 9-12).

The die 10 also has a bottom side 16 that supports a bottom side thermal metallization 17 (see page 4, lines 19-20). The bottom side thermal metallization 17 defines a thermal contact area on the bottom side 16 of the die 10 that provides a high thermal conductivity path from the die to, for example, a heat spreader of a package into which die 10 will be mounted (see page 4, lines 20-23).

Figures 3, 4A and 4B show an embodiment of a method of making an integrated circuit system in accordance with the invention defined in independent claim 15. In accordance with this inventive method, multiple die regions 10 are formed on a top side of a substrate 50 (e.g., a semiconductor wafer) (block 52; see page 6, lines 30-32 of the specification). The die regions 10 that are formed on substrate 50 are separated from one another by street areas 54. Each die region 10 has an electrical signal communication metallization 18 and a top side thermal dissipation metallization 20, as described in detail above. A bottom side thermal dissipation metallization 17 is formed on a bottom side of the substrate 50 for each die region (block 56; see page 7, lines 2-4). The bottom side thermal dissipation metallization 17 may be formed as a uniform layer or layers of metal that are deposited onto the bottom side of the substrate 50, as shown in FIG. 4B. Alternatively, the bottom side thermal dissipation metallization 17 may be patterned using, for example, photolithographic processing techniques. The die regions 10 are singulated to form respective integrated circuit dice (block 58; see page 7, lines 8 and 9). As shown in FIG. 1A, the

bonding elements of the electrical signal communication metallization 18 are disposed on the top side 14 of die 10 in a peripheral region 22 in accordance with the aspect of the invention defined in claims 3 and 6 (see page 4, lines 25-27). The top side thermal dissipation metallization 20 is disposed on the top side of die 10 within a central region 28 surrounded by the peripheral region 22 in accordance with the aspect of the invention defined in claims 4 and 5 (see page 4, lines 31-33).

Figures 5A and 5B show an embodiment of an integrated circuit die 60 that includes a top side thermal dissipation metallization 62 that has an array of through-holes 64 in accordance with the aspect of the invention defined in claims 8 and 9. These through-holes help to reduce stress buildup in the integrated circuit die 60 (see page 7, lines 18-21).

VI. Grounds of Rejection to be Reviewed on Appeal

A. Claims 1-9 and 21 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Hideshima et al. (U.S. 5,143,865) in view of Wu (U.S. 2003/0067057).

B. Claims 1-4 and 6-11 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Hideshima et al. (U.S. 5,143,865) in view of Kunikiyo (U.S. 6,717,267).

C. Claims 12 and 13 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Hideshima et al., Kunikiyo, and Wang (US. 5,977,626).

D. Claim 14 stands rejected under 35 U.S.C. § 103(a) as unpatentable over Hideshima et al., Kunikiyo, and Khan (U.S. 6,853,070).

E. Claims 15-18 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Hideshima et al. in view of White (U.S. 5,665,655) and Kunikiyo.

F. Claims 19 and 20 are rejected under 35 U.S.C. § 103(a) as unpatentable over Hideshima et al. in view of White, Kunikiyo, and Wang.

VII. Argument

A. Rejection of Claims 1-9 and 21 Under 35 U.S.C. § 103(a) as Unpatentable Over Hideshima et al. (U.S. 5,143,865) in View of Wu (U.S. 2003/0067057)

Claims 1-9 and 21 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Hideshima et al. (U.S. 5,143,865) in view of Wu (U.S. 2003/0067057). It is respectfully submitted that these claims would not have been obvious to a person of ordinary skill in the art for at least the reasons that these references neither collectively disclose all claim limitations nor provide any motivation or suggestion for combining their teachings in a manner that arrives at the invention as it is recited in these claims.

Independent Claim 1

Hideshima et al. discloses a semiconductor structure having solder bumps formed on one side and a metal layer (16) and solder layer (41, 43, 45) formed on the other side. In rejecting independent claim 1, the Examiner acknowledged that Hideshima et al. "does not disclose a top side thermal dissipation metallization." (See Office Action dated May 7, 2007, page 2, ¶ 3, line 5.) However, the Examiner took the position that Wu discloses this feature as well as a reason why a person of ordinary skill in the art would have been motivated to include this feature in a structure such as that disclosed by Hideshima et al. et al:

> Nevertheless, Wu (e.g. fig. 3A) shows a die a [sic] topside thermal dissipation metallization 21. This type of embodiment allows the heat generated from a semiconductor chip to be quickly dissipated through a die pad of the lead frame after the semiconductor chip is attached to the die pad, so as to improve overall heat dissipating efficiency of the semiconductor package (pp 0009). . . .

(Office Action dated May 7, 2007; pages 2-3, ¶ 3, lines 5-10.)

In FIG. 3A, Wu shows a semiconductor package 2 that includes a semiconductor chip (or die) 23 that is bonded to a lead frame and is encapsulated by an encapsulant 25. The lead frame has leads 222 and a die pad 21, which are formed by a half-etching process (see ¶ 34, line 5 and lines 15-20). Solder bumps 24 bond contact pads on the active surface 230 of the semiconductor chip 23 to the leads 222, and a non-conductive thermal adhesive 212 bonds the active surface 230 of the semiconductor chip 23 to the die pad 21.

Contrary to the Examiner's statement, the die pad 21 of Wu does not constitute a top side thermal dissipation metallization that is supported on the top side of the semiconductor

chip 23. First, the die pad 21 is not a "metallization" as defined in the specification. On page 4, lines 3-4, the specification recites: "As used herein, the term 'metallization' refers to single-layer metal film or a multi-layer metal film formed in or on an integrated circuit." The formation of such films or metal layers using integrated circuit fabrication technology is well understood in the art. Persons skilled in the art readily understand what a metal film or layer is in the context of integrated circuit technology. The die pad 21 of Wu does not constitute a single-layer metal film or a multi-layer metal film. Rather, the die pad 21 is an integral component of a package lead frame that is adhesively bonded to the semiconductor chip 23 only when the semiconductor chip 23 is mounted in the package 2 (see FIG. 2B, which shows the die pad 110 as an integral component of the lead frame 10), not a film. Thus, one skilled in the art at the time the invention was made would not have considered the die pad 21 to be a "thermal dissipation metallization" as recited in claim 1.

Second, there is no reasonable interpretation of the word "supporting" in the recitation of the top side "supporting an electrical signal communication metallization and a top side thermal dissipation metallization" that could read on the die pad 21 of Wu. The die pad 21 does no more than hold the semiconductor chip 23 ("stopped from moving") and space it from leads 22 during the process of reflowing the solder bumps 24 (see, e.g., ¶ 34, lines 10-15; see also ¶ 31). Third, Wu discloses that the bonding pads are the only elements that are supported on the top side of the semiconductor chip 23 (see, e.g., FIG. 3A). One skilled in the art at the time the invention was made reasonably would infer from this disclosure, that the top surface of the semiconductor chip 23 is devoid of any type of structural elements designed to dissipate heat through the adhesive 212 and the die pad 21.

In summary, neither Hideshima et al. nor Wu teaches anything about a die that has a top side supporting top side thermal dissipation metallization as recited in claim 1. Therefore, the combination of Hideshima et al. and Wu cannot possibly teach or suggest the invention defined by independent claim 1. For at least this reason, it is respectfully requested that the Board reverse the Examiner's rejection of independent claim 1 under 35 U.S.C. § 103(a) as unpatentable over Hideshima et al. in view of Wu.

The rejection of claim 1 under 35 U.S.C. § 103(a) as unpatentable over Hideshima et al. in view of Wu also should be withdrawn because this rejection relies on an impermissible hindsight reconstruction of the invention. As an alleged reason why a person of ordinary skill in the art would have made the combination, the Examiner stated:

It would have been obvious to one of ordinary skill in the art at the time the

> invention was made to form a top side thermal dissipation metallization layer as disclosed by Wu to allow the heat generated from a semiconductor chip to be quickly dissipated through a die pad of the lead frame after the semiconductor chip is attached to the die pad, so as to improve overall heat dissipating efficiency of the semiconductor package as suggested by Wu.

(Office Action dated May 7, 2007, page 3, ¶ 3, line 10 to page 4, ¶ 3, line 2.).

This rationale, however, is insufficient to establish a *prima facie* case of obviousness under 35 U.S.C. § 103.

First, the Examiner's rationale is not based on a suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings. (See the first prong of the test explained in MPEP § 706.02(j).) In particular, neither Hideshima et al. nor Wu teaches or suggests anything about supporting thermal dissipation metallizations on both top and bottom sides of a die. In accordance with Hideshima et al.'s teaching, only the bottom side of the semiconductor chip supports a thermal dissipation metallization (i.e., the solder layer 45C). Putting aside the fact that Wu does not teach that the semiconductor chip 23 has any side that supports a thermal dissipation metallization, heat is dissipated out of the semiconductor chip 23 primarily through the active surface 230 of the semiconductor chip 23 via the non-conductive thermal adhesive 212 and the lead frame. Thus, neither Hideshima et al. nor Wu teaches or suggests anything about supporting thermal dissipation metallizations on both top and bottom sides of a die. Therefore, one skilled in the art at the time the invention was made would not have had any motivation to modify Hideshima et al.'s teachings in the manner proposed by the Examiner.

Second, one skilled in the art at the time the invention was made would not have had a reasonable expectation that the Examiner's proposed modification of Hideshima et al.'s teachings would be successful (see the first prong of the test explained in MPEP § 706.02(j)). The Examiner's position is that one skilled in the art would have been motivated to attach the die pad 21 disclosed in Wu to the top side of the semiconductor chip 10 disclosed in Hideshima et al. As explained above, however, the die pad 21 and the leads 222 are integral components of the lead frame (see, e.g., FIG. 2B of Wu). Therefore, it would not be possible to simply attach the die pad 21 of Wu to the central portion of the top side of the semiconductor chip 10 of Hideshima et al. without the other portions of the lead frame. As shown in FIG. 4 of Hideshima et al., however, such a modification would short-circuit the emitter regions 13 and the collector electrode 16 in Hideshima et al.'s semiconductor chip

(see, e.g., FIG. 8). The fact is that the semiconductor chips disclosed in Hideshima et al. and Wu have different electrical connection needs. As a result, one skilled in the art would have to modify of the teachings of both references in ways that neither reference teaches or suggests in order to arrive at the inventive integrated circuit system as it is defined in claim 1.

For the reasons explained above, it appears that the Examiner impermissibly engaged in hindsight reconstruction of the claimed invention, using Applicants' own disclosure as a blueprint for piecing together the cited prior art to defeat patentability. Without a proper explanation for combining the cited prior art to arrive at the invention recited in claim 1, the Examiner has failed to establish a proper prima facie case of obviousness, and the rejection of claim 1 should be reversed for this additional reason.

Dependent Claims 2-9 and 21

Each of claims 2-9 and 21 incorporates the features of independent claim 1 and therefore is patentable over Hideshima et al. and Wu for at least the same reasons explained above. Claims 8 and 9 also are patentable over Hideshima et al. and Wu for the following additional reasons.

Claim 8:

As set forth in claim 8, which further depends from claim 7, the patterned metal layer of the top side thermal dissipation metallization comprises at least one through-hole. The Examiner stated that "Hideshima shows that the patterned metal layer comprises at least one through-hole" (see page 3, ¶ 11 of the Office action). In the rejection of claim 1, however, the Examiner took the position that the die pad 21 shown in FIG. 3A constitutes a top side thermal dissipation that is supported by the top surface of the semiconductor chip 23. As shown clearly in FIG. 3A, the die pad 21 does not include at least one through-hole. For at least this additional reason, the Examiner's rejection of claim 8 under 35 U.S.C. § 103(a) over Hideshima et al. in view of Wu should be reversed.

Claim 9:

Claim 9 depends from claim 8 and recites that the patterned metal layer comprises an array of through-holes. Claim 9 is patentable over Hideshima et al. and Wu for essentially the same additional reasons explained above in connection with claim 8. As the die pad 21 does not have a through-hole, it does not have an array of through-holes.

B. Rejection of Claims 1-4 and 6-11 Under 35 U.S.C. § 103(a) as Unpatentable Over Hideshima et al. (U.S. 5,143,865) in View of Kunikiyo (U.S. 6,717,267)

Claims 1-4 and 6-11 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Hideshima et al. (U.S. 5,143,865) in view of Kunikiyo (U.S. 6,717,267). It is respectfully submitted that these claims would not have been obvious to a person of ordinary skill in the art for at least the reasons that these references neither collectively disclose all claim limitations nor provide any motivation or suggestion for combining their teachings in a manner that arrives at the invention as it is recited in these claims.

Independent Claim 1

Hideshima et al. discloses a semiconductor structure having solder bumps formed on one side and a metal layer (16) and solder layer (41, 43, 45) formed on the other side. In rejecting independent claim 1, the Examiner acknowledged that Hideshima et al. "does not disclose a top side thermal dissipation metallization." (See Office Action dated May 7, 2007, page 2, ¶ 3, line 5). However, the Examiner took the position that Kunikiyo discloses this feature as well as a reason why a person of ordinary skill in the art would have been motivated to include this feature in a structure such as that disclosed in Hideshima et al.

> Nevertheless, Kunikiyo (e.g. fig. 19) shows a top side thermal dissipation metallization 31. According to Kunikiyo, this type of mounting structure provides more satisfactory effect of cooling away the heat in the interlayer insulating films than conventional semiconductor devices having no dummy interconnections or dummy plugs, since metal has higher thermal conducting rate than the interlayer insulating films. This improves the circuit operation of the semiconductor device (col. 23/lls. 1-18) . . . .

(Office Action dated May 7, 2007, page 4, ¶ 14, lines 6-11.)

In FIG. 19, Kunikiyo discloses a semiconductor device that includes dummy interconnections 9a-b, 21a-c, and 25a-c, dummy plugs 22a-b, 26a-c, 29b-c, and 31, and a heat sink 32. The dummy interconnections are formed in order to improve the flatness in the CMP processes used in the formation of the semiconductor device and to correct the proximity effect in which the finished resist form is affected by the proximate pattern form in the transfer processes used in the formation of the semiconductor device. (See Kunikiyo, col. 5, lines 46-50.) The dummy plugs 22a-b, 26a-c, and 29b-c serve to connect the dummy interconnections to ground potential in order to reduce noise. (See, e.g., col. 10, lines 28-38.) The dummy plugs 31 serve to transfer heat from the interlayer insulating films to the heat

sink 32, which dissipates the heat.

Contrary to the Examiner's statement, the dummy plugs 31 do not constitute a "thermal dissipation metallization."

First, the dummy plugs 31 do not constitute a "metallization" as defined in the specification. On page 4, lines 3-4, the specification of the instant application states: "As used herein, the term "metallization" refers to single-layer metal film or a multi-layer metal film formed in or on an integrated circuit." The dummy plugs 31 do not constitute a single-layer metal film or a multi-layer metal film. Instead, the dummy plugs 31 constitute a small number of spaced-apart metal plugs that are positioned only where the dummy interconnections are located and are formed by filling through-holes in the passivation film 30 with metal and chemically-mechanically removing excess metal until the top surfaces of the plugs 31 and the passivation film 30 coincide. (See, e.g., FIG. 19 and col. 11, line 36 - col. 12, line 23.)

Second, the dummy plugs 31 do not constitute a "thermal dissipation" metallization in accordance with the ordinary and accustomed meaning of the term "thermal dissipation." In accordance with its ordinary and accustomed meaning, the word "dissipation" refers to the action or process of breaking up and driving off or causing to spread thin or scatter and gradually vanish. (See, e.g., Merriam-Webster's Collegiate Dictionary, 10th ed.). A commonly understood definition of "thermal" is "of, relating to, or caused by heat." (See, e.g., Merriam-Webster's Collegiate Dictionary, 10th ed.). The dummy plugs 31 do not break up and drive off heat nor do they cause heat to spread thin or scatter and gradually vanish. Instead, the dummy plugs 31 merely conduct heat from the regions of the interlayer insulating films near the dummy interconnections to the heat sink 32, which dissipates the heat.

Thus, one skilled in the art at the time the invention was made reasonably would not have considered the dummy plugs 31 to be a "thermal dissipation metallization" as recited in claim 1. Since neither Hideshima et al. nor Kunikiyo teaches or suggests anything about a die that has a top side supporting top side thermal dissipation metallization as recited in claim 1, the combination of Hideshima et al. and Kunikiyo cannot possibly teach or suggest the invention defined by independent claim 1. For at least this reason, the rejection of independent claim 1 under 35 U.S.C. § 103(a) over Hideshima et al. and Kunikiyo should be reversed.

The rejection of claim 1 under 35 U.S.C. § 103(a) over Hideshima et al. in view of Kunikiyo also should be reversed because this rejection relies on an impermissible hindsight

reconstruction of the invention. As an alleged reason why a person of ordinary skill in the art would have made the combination, the Examiner stated:

> It would have been obvious to one of ordinary skill in the art at the time the invention was made to include in Hideshima's invention a topside thermal dissipation metallization such as dummy patterns in accordance to Kunikiyo's invention to improve the circuit operation since the heat can be satisfactorily removed form the interlayer insulating films.

(Office Action dated May 7, 2007, page 4, ¶ 14, lines 12- 16.)

This rationale, however, is insufficient to establish a *prima facie* case of obviousness under 35 U.S.C. § 103.

First, the Examiner's rationale is not based on a suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings. (See the first prong of the test explained in MPEP § 706.02(j).)

Neither Hideshima et al. nor Kunikiyo teaches or suggests anything about supporting thermal dissipation metallizations on both top and bottom sides of a die. In accordance with Hideshima et al.'s teaching, only the bottom side of the semiconductor chip supports a thermal dissipation metallization (i.e., the solder layer 45C). Putting aside the fact that Kunikiyo does not teach that the semiconductor device shown in FIG. 19 has any side that supports a thermal dissipation metallization, heat is dissipated out of the semiconductor device only through the top side of the semiconductor device via the heat sink 32. Thus, neither Hideshima et al. nor Kunikiyo teaches or suggests anything about supporting thermal dissipation metallizations on both top and bottom sides of a die. Therefore, one skilled in the art at the time the invention was made would not have had any motivation to modify Hideshima et al.'s teachings in the manner proposed by the Examiner.

Furthermore, neither Hideshima et al. nor Kunikiyo teaches or suggest anything that would have led one skilled in the art at the time the invention was made to incorporate a structure along the lines of Kunikiyo's dummy plugs 31 in the insulating film 17 of Hideshima et al.'s semiconductor device 10, as proposed by the Examiner. Hideshima et al. does not teach or suggest anything about the desirability of a heat-conducting connecting structure along the lines of dummy plugs and dummy interconnections. In accordance with Kunikiyo's teachings, the dummy plugs 31 only serve to connect the underlying dummy interconnections to the heat sink 32. Since there are no dummy interconnections in Hideshima et al.'s semiconductor device 10, one skilled in the art would not have had any motivation to

incorporate the dummy plugs 10 or anything similar in Hideshima et al.'s semiconductor device.

Second, one skilled in the art at the time the invention was made would not have had a reasonable expectation that the Examiner's proposed modification of Hideshima et al.'s teachings would be successful. (See the first prong of the test explained in MPEP § 706.02(j).) The Examiner's position is that one skilled in the art would have been motivated to incorporate Kunikiyo's plugs 31 in the insulating film 17 on the top side of Hideshima et al.'s semiconductor chip 10. As explained above, however, the dummy plugs 31 only serve to connect the underlying dummy interconnections to the heat sink 32, which covers the entire top surface of Kunikiyo's semiconductor device, as shown in FIG. 19. It would not be possible to attach a heat sink of the type disclosed in Kunikiyo on the top side of Hideshima et al.'s semiconductor chip 10 because, as shown in FIG. 4 of Hideshima et al., such a modification would interfere with the interconnection between the lead frame and the solder bumps on the top surface of Hideshima et al.'s semiconductor chip 10. (See Hideshima et al., FIG. 8). The semiconductor chips disclosed in Hideshima et al. and Kunikiyo have different electrical connection needs. As a result, one skilled in the art would have had to modify of the teachings of both references in a way that neither reference teaches or suggests and that would not have been within the general knowledge of one of ordinary skill in the art in order to arrive at the inventive integrated circuit system as it is defined in claim 1.

For the reasons explained above, it appears that the Examiner impermissibly engaged in hindsight reconstruction of the claimed invention, using Applicants' own disclosure as a blueprint for piecing together the cited prior art to defeat patentability. Without a proper explanation for combining the cited prior art to arrive at the invention recited in claim 1, the Examiner has failed to establish a proper prima facie case of obviousness, and the rejection of claim 1 should be reversed for this additional reason.

Dependent Claims 2-4 and 6-11

Each of claims 2-4 and 6-11 incorporates the features of independent claim 1 and therefore is patentable over Hideshima et al. and Kunikiyo for at least the same reasons explained above. Claims 8-11 also are patentable over Hideshima et al. and Kunikiyo for the following additional reasons.

Claim 8:

Claim 8 recites that the patterned metal layer comprises at least one through-hole.

The Examiner stated that "Hideshima shows that the patterned metal layer comprises at least one through-hole." (Office Action dated May 7, 2007, page 5, ¶ 20). In rejecting claim 1, the Examiner took the position that the die pad 21 shown in FIG. 3A of Hideshima et al. constitutes a top side thermal dissipation that is supported by the top surface of the semiconductor chip 23. As shown clearly in FIG. 3A, there is no through-hole in die pad 21. For at least this additional reason, the rejection of claim 8 under 35 U.S.C. § 103(a) as unpatentable over Hideshima et al. in view of Kunikiyo should be reversed.

Claim 9:

Claim 9 depends from claim 8 and additionally recites that the patterned metal layer comprises an array of through-holes. Claim 9 is patentable over Hideshima et al. and Kunikiyo for essentially the same additional reasons explained above in connection with claim 8. As die pad 21 does not have a through-hole, it does not have an array of through-holes.

Claim 10:

Claim 10 depends from claim 1 and additionally recites that the integrated circuit system includes a package comprising a top heat spreader metallurgically bonded to the top side thermal dissipation metallization of the die. In rejecting claim 10, the Examiner stated that Kunikiyo "shows a top heat spreader 32 metallurgically bonded to the top side thermal dissipation metallization of the die." (Office Action dated May 7, 2007, page 5, ¶ 18.) Kunikiyo discloses attaching a heat sink 32 to plugs 31 that are formed in a passivation film 30. (See Kunikiyo, col. 23, lines 1-18). Kunikiyo, however, does not teach or suggest any specific means by which the heat sink 32 is attached to the plugs 31. Therefore, there is no support for the Examiner's proposed combination of the heat sink 32 being metallurgically bonded to the plugs 31. For at least these additional reasons the Examiner's rejection of claim 10 under 35 U.S.C. § 103(a) as unpatentable over Hideshima et al. in view of Kunikiyo should be withdrawn.

Claim 11 depends from claim 10 and therefore is patentable over Hideshima et al. and Kunikiyo for at least the same reasons.

C. Rejection of Claims 12 and 13 Under 35 U.S.C. § 103(a) as Unpatentable Over Hideshima et al. (U.S. 5,143,865) in View of Kunikiyo (U.S. 6,717,267), and Further in View of Wang (US. 5,977,626)

Claims 12 and 13 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Hideshima et al. in view of Kunikiyo, and further in view of Wang (U.S. 5,977,626). It is respectfully submitted that these claims would not have been obvious to a person of ordinary skill in the art for at least the reasons that these references neither collectively disclose all claim limitations nor provide any motivation or suggestion for combining their teachings in a manner that arrives at the invention as it is recited in these claims.

Each of claims 12 and 13 incorporates the features of claim 10. As discussed above with regard to the rejection of claim 10, claim 10 additionally recites that the integrated circuit system includes a package comprising a top heat spreader metallurgically bonded to the top side thermal dissipation metallization of the die. In rejecting claim 10, the Examiner stated that Kunikiyo "shows a top heat spreader 32 metallurgically bonded to the top side thermal dissipation metallization of the die." (Office Action dated May 7, 2007, page 5, ¶ 18.) As also discussed above, Kunikiyo does not disclose anything about the means by which the heat sink 32 is attached to the plugs 31. Wang does not disclose such a feature. Indeed, Wang teaches that the heat spreader 32 is attached to the top side of the die 22 using an adhesive, such as a heat spreader attach epoxy. (Wang, col. 3, lines 49-53.) As none of Hideshima et al., Kunikiyo or Wang teaches or suggest the features discussed above in connection with claim 10, claim 10 and the claims that depend therefrom could not have been obvious to a person of ordinary skill in the art.

For at least these reasons the rejection of claims 12 and 13 under 35 U.S.C. § 103(a) as unpatentable over Hideshima et al. in view of Kunikiyo, and further in view of Wang should be reversed.

D. Rejection of Claim 14 Under 35 U.S.C. § 103(a) as Unpatentable Over Hideshima et al. (U.S. 5,143,865) in View of Kunikiyo (U.S. 6,717,267), and Further in View of Khan (US. 6,853,070)

Claim 14 stands rejected under 35 U.S.C. § 103(a) as unpatentable over Hideshima et al. in view of Kunikiyo, and further in view of Khan (U.S. 6,853,070). Claim 14 incorporates

the features of independent claim 10. As discussed above with regard to the rejection of claim 10, claim 10 additionally recites that the integrated circuit system includes a package comprising a top heat spreader metallurgically bonded to the top side thermal dissipation metallization of the die. As also discussed above, Kunikiyo does not disclose anything about the means by which the heat sink 32 is attached to the plugs 31. Khan does not disclose such a feature. Indeed, Khan clearly teaches that the drop-in heat spreader 202 is attached to the top side of the die 102 using an epoxy 204. (Khan, FIG. 2A and col. 7, lines 29- 31.) Khan fails to teach or suggest anything about a top side thermal dissipation metallization.

For at least these reasons the Examiner's rejection of claim 14 under 35 U.S.C. § 103 (a) over Hideshima et al. in view of Kunikiyo and Khan should be withdrawn. The Examiner's rejection of claim 14 also should be withdrawn for the following additional reasons.

Claim 14 recites that the package further comprises a bottom heat spreader metallurgically bonded to the bottom side thermal dissipation metallization of the die. The Examiner stated that "Khan (e.g., fig. 2A) shows a bottom heat spreader 110 bonded to the bottom side thermal dissipation metallization of the die 102." (Office Action dated May 7, 2007, page 6, ¶ 28, lines 4-5.) Khan, however, teaches that the heat spreader 110 is attached to the bottom side of the die 102 using an epoxy. (See Khan, col. 4, lines 60-61). In addition, contrary to the Examiner's assumption, Khan does not teach or suggest that the die 102 includes a bottom side thermal dissipation metallization.

For at least these additional reasons, the rejection of claim 14 under 35 U.S.C. § 103(a) as unpatentable over Hideshima et al. in view of Kunikiyo, and further in view of Khan should be reversed.

E. Rejection of Claims 15-18 Under 35 U.S.C. § 103(a) as Unpatentable Over Hideshima et al. (U.S. 5,143,865) in View of White (U.S. 5,665,655), and Further in View of Kunikiyo (U.S. 6,717,267)

Claims 15-18 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Hideshima et al. in view of White (U.S. 5,665,655), and further in view of Kunikiyo. It is respectfully submitted that these claims would not have been obvious to a person of ordinary skill in the art for at least the reasons that these references neither collectively disclose all claim limitations nor provide any motivation or suggestion for combining their teachings in a manner that arrives at

the invention as it is recited in these claims.

Independent Claim 15

Independent claim 15 relates to a method making a integrated circuit system of the type recited in, for example, claim 1. The process is performed at a wafer level, i.e., features are formed on a common substrate that define individual die regions, and the die regions are then singulated to form individual integrated circuit dice. The Examiner cited White merely for teaching "a method including the steps of forming multiple die regions on a substrate and the step of . . . singulating the die regions to form the integrated circuit . . . [dice]." However, that singulation of a substrate is, in and of itself, known in the art does not bear upon the absence of any teaching or suggestion in Hideshima et al. or Kunikiyo of the pertinent features of the integrated circuit system itself, discussed above with regard to the rejection of claim 1. With specific reference to claim 15, neither Hideshima et al. nor Kunikiyo teaches or suggests at least "forming on a top side of a substrate . . . an exposed top side thermal dissipation metallization . . . ." Therefore, claim 15 is patentable over Hideshima et al., White and Kunikiyo for at least the same reasons explained above in connection with independent claim 1.

Dependent Claims 16-18

Each of claims 16-18 depends from and thus incorporates the features recited in independent claim 15 and therefore is patentable over Hideshima et al., White, and Kunikiyo for at least the same reasons explained above. Claim 18 also is patentable over Hideshima et al., White, and Kunikiyo for the following additional reasons.

Claim 18:

In rejecting claim 18, the Examiner stated that "Kunikiyo (e.g. fig. 19) shows the step of metallurgically bonding a top heat spreader of the package (e.g. 31) to the top side thermal dissipation metallization of the singulated die (dummy pattern 25a)." (Office Action dated May 7, 2007, page 9, ¶ 33. Kunikiyo, however, does not teach or suggest any specific means by which the heat sink 32 is attached to the plug 31. Therefore, there is no support for the Examiner's assertion that the heat sink 32 is metallurgically bonded to the plug 31.

For at least these additional reasons, the Examiner's rejection of claim 18 under 35 U.S.C. § 103(a) as unpatentable over Hideshima et al. in view of White, and further Kunikiyo should be reversed.

F. Rejection of Claims 19 and 20 Under 35 U.S.C. § 103(a) as Unpatentable Over Hideshima et al. (U.S. 5,143,865) in View of White (U.S. 5,665,655) and Kunikiyo (U.S. 6,717,267), and Further in View of Wang (U.S. 5,977,626)

Claims 19 and 20 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Hideshima et al. in view of White and Kunikiyo, and further in view of Wang. Each of claims 19 and 20 depends from and thus incorporates the features recited in claim 18. As discussed above with regard to the rejection of claim 18, Kunikiyo does not teach or suggest anything about attaching the heat sink 32 to the plug 31. Therefore, there is no support for the Examiner's assertion that the heat sink 32 is metallurgically bonded to the plug 31. Wang does not disclose such a feature. Indeed, Wang teaches that the heat spreader 32 is attached to the top side of the die 22 using an adhesive, such as a heat spreader attach epoxy (see col. 3, lines 49-53). Wang does not teach or suggest anything about either a top side thermal dissipation metallization or a back side thermal dissipation metallization.

As none of White, Kunikiyo and Wang teaches or suggests the feature recited in claim 18, from which claims 19 and 20 depend, the Examiner's rejection of claims 19 and 20 under 35 U.S.C. § 103(a) as unpatentable over Hideshima et al. in view of White, Kunikiyo, and Wang should be reversed.

VIII. Conclusion

For the reasons explained above, Appellant respectfully submits that the rejections set forth in the final Office Action dated May 7, 2007, are without merit, and therefore respectfully requests that the honorable Board reverse the rejections.

Respectfully submitted,

Smith Frohwein Tempel Greenlee Blaha LLC
Customer No. 35856

By: /Lawrence D. Maxwell/
Lawrence D. Maxwell, Reg. No. 35,276
(770) 709-0085

CLAIMS APPENDIX

Claim 1 (original): An integrated circuit system, comprising:

a die incorporating an integrated circuit and having a top side and a bottom side, the top side supporting an electrical signal communication metallization and a top side thermal dissipation metallization, and the bottom side supporting a bottom side thermal dissipation metallization.

Claim 2 (previously presented): The system of claim 1, wherein the electrical signal communication metallization comprises a plurality of exposed bonding elements on the top side of the side.

Claim 3 (previously presented): The system of claim 2, wherein the bonding elements are contained in a peripheral region on the top side of the die.

Claim 4 (previously presented): The system of claim 3, wherein the top side thermal dissipation metallization is contained in a central region on the top side of the die.

Claim 5 (previously presented): The system of claim 4, wherein the top side thermal dissipation metallization is surrounded by the plurality of bonding elements.

Claim 6 (previously presented): The system of claim 1, wherein the electrical signal communication metallization surrounds the top side thermal dissipation metallization.

Claim 7 (original): The system of claim 1, wherein the top side thermal dissipation metallization comprises a patterned metal layer.

Claim 8 (original): The system of claim 7, wherein the patterned metal layer comprises at least one through-hole.

Claim 9 (original): The system of claim 8, wherein the patterned metal layer comprises an array of through-holes.

Claim 10 (original): The system of claim 1, further comprising a package comprising a top heat spreader metallurgically bonded to the top side thermal dissipation metallization of the die.

Claim 11 (original): The system of claim 10, wherein the integrated circuit is connected electrically to the top side heat spreader by an electrical path extending through the top side thermal dissipation metallization.

Claim 12 (original): The system of claim 10, wherein the package further comprises an electrical interface and a substrate containing a wiring interconnection between the electrical signal communication metallization and the electrical interface.

Claim 13 (original): The system of claim 12, wherein the top heat spreader is mounted on the substrate and forms a lid of the package covering the top side of the die.

Claim 14 (original): The system of claim 10, wherein the package further comprises a bottom heat spreader metallurgically bonded to the bottom side thermal dissipation metallization of the die.

Claim 15 (previously presented): A method of making an integrated circuit system, comprising:

forming on a top side of a substrate multiple die regions each having a top side supporting an exposed electrical signal communication metallization and an exposed top side thermal dissipation metallization;

forming on a bottom side of the substrate an exposed bottom side thermal dissipation metallization for each die region; and

singulating the die regions to form respective integrated circuit dice.

Claim 16 (previously presented): The method of claim 15, wherein, in each die region, the electrical signal communication metallization surrounds the top side thermal dissipation metallization.

Claim 17 (previously presented): The method of claim 15, wherein each top side thermal dissipation metallization comprises an exposed metal layer with an array of through-holes.

Claim 18 (original): The method of claim 15, further comprising mounting each singulated die in a respective package having a top heat spreader, wherein mounting a singulated die comprises metallurgically bonding the top heat spreader of a package to the top side thermal dissipation metallization of the singulated die.

Claim 19 (original): The method of claim 18, wherein the package additionally includes a substrate and mounting the singulated die further comprises mounting the package substrate to the bottom side thermal dissipation metallization of the singulated die.

Claim 20 (original): The method of claim 18, wherein the top heat spreader is mounted on the substrate and forms a lid of the package, and further comprising encapsulating the die within the package with an encapsulating material.

Claim 21 (previously presented): The system of claim 1, wherein the electrical signal communication metallization is free of any direct electrical connection to the top side thermal dissipation metallization on the top of the die.

EVIDENCE APPENDIX

There is no evidence submitted pursuant to 37 C.F.R. §§ 1.130, 1.131 or 1.132, or any other evidence entered by the Examiner and relied upon by Appellant in the pending appeal.

RELATED PROCEEDINGS APPENDIX

Appellant is not aware of any decisions rendered by a court or the Board that will directly affect or be directly affected by or have a bearing on the Board's decision in this pending appeal.